UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

MLC INTELLECTUAL PROPERTY, LLC,
Plaintiff,
v.
MICRON TECHNOLOGY, INC.,
Defendant.

Case No. 14-cv-03657-SI

ORDER RE: CLAIM CONSTRUCTION

Re: Dkt. Nos. 72, 75, 76

On September 28, 2016, the Court held a tutorial and claim construction hearing. After consideration of the record and the parties' arguments, the Court enters this claim construction order.

BACKGROUND

On August 12, 2014, plaintiff MLC Intellectual Property, LLC brought suit against defendant Micron Technology, Inc., alleging infringement of United States Patent No. 5,764,571 ("the '571 patent"). Dkt. No. 1. The '571 patent is entitled "Electrically Alterable Non-Volatile Memory with n-bits Per Cell." The '571 patent discloses non-volatile memory devices and methods of programming and/or verifying the programming of multi-level non-volatile memory devices. Non-volatile memory is capable of retaining the data with which it is programmed after the device is powered off. *See* '571 Patent 1:19-18; Dkt. No. 72-2 at ¶ 16. The memory device, made up of multiple semiconductor cells, has K^n predetermined memory states, where K is a base of a predetermined number system (such as 2 in the binary system of "1" or "0"), n is the number

of bits that can be stored in each cell, and $K^n > 2$. '571 Patent at abstract.

Conventional memory cell devices allowed only two memory storage states in each cell based on the one bit of information the cell was capable of storing. *Id.* at 1:24-26. Memory storage devices that were enhanced to allow multiple bits of storage per cell were either non-alterable read-only-memory systems or volatile memory devices not capable of permanent storage. *Id.* at 1:31-35. The '571 patent attempts to solve this drawback by creating a "multi-level electrically alterable non-volatile memory (EANVM) device, wherein some or all of the storage locations have more than two states." *Id*. at 2:50-54.

LEGAL STANDARD

Claim construction is a matter of law. *Markman v. Westview Instr., Inc*., 517 U.S. 370, 372 (1996). Terms contained in claims are "generally given their ordinary and customary meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id*. at 1312. In determining the proper construction of a claim, a court begins with the intrinsic evidence of record, consisting of the claim language, the patent specification, and, if in evidence, the prosecution history. *Id*. at 1313; *see also Vitronics Corp. v. Conceptronic, Inc*., 90 F.3d 1576, 1582 (Fed. Cir. 1996). "The appropriate starting point . . . is always with the language of the asserted claim itself." *Comark Communications, Inc. v. Harris Corp*., 156 F.3d 1182, 1186 (Fed. Cir. 1998); *see also Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed. Cir. 1997).

Accordingly, although claims speak to those skilled in the art, claim terms are construed in light of their ordinary and accustomed meaning, unless examination of the specification, prosecution history, and other claims indicates that the inventor intended otherwise. *See Electro Medical Systems, S.A. v. Cooper Life Sciences, Inc*., 34 F.3d 1048, 1053 (Fed. Cir. 1994). The written description can provide guidance as to the meaning of the claims, thereby dictating the manner in which the claims are to be construed, even if the guidance is not provided in explicit definitional format. *SciMed Life Systems, Inc. v. Advanced Cardiovascular Systems, Inc*., 242

F.3d 1337, 1344 (Fed. Cir. 2001). In other words, the specification may define claim terms "by implication" such that the meaning may be "found in or ascertained by a reading of the patent documents." *Vitronics*, 90 F.3d at 1584 n.6.

In addition, the claims must be read in view of the specification. *Markman v. Westview Instr., Inc.*, 52 F.3d 967, 978 (Fed. Cir. 1995). Although claims are interpreted in light of the specification, this "does not mean that everything expressed in the specification must be read into all the claims." *Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 957 (Fed. Cir. 1983). For instance, limitations from a preferred embodiment described in the specification generally should not be read into the claim language. *See Comark*, 156 F.3d at 1187. However, it is a fundamental rule that "claims must be construed so as to be consistent with the specification." *Phillips*, 415 F.3d at 1316. Therefore, if the specification reveals an intentional disclaimer or disavowal of claim scope, the claims must be read consistently with that limitation. *Id.*

Finally, the Court may consider the prosecution history of the patent, if in evidence. *Markman*, 52 F.3d at 980. The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution. *See Southwall Technologies, Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995). In most situations, analysis of this intrinsic evidence alone will resolve claim construction disputes. *See Vitronics*, 90 F.3d at 1583. Courts should not rely on extrinsic evidence in claim construction to contradict the meaning of claims discernable from examination of the claims, the written description, and the prosecution history. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1308 (Fed. Cir. 1999) (citing *Vitronics*, 90 F.3d at 1583). However, it is entirely appropriate "for a court to consult trustworthy extrinsic evidence to ensure that the claim construction it is tending to from the patent file is not inconsistent with clearly expressed, plainly apposite, and widely held understandings in the pertinent technical field." *Id.* Extrinsic evidence "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317. All extrinsic evidence should be evaluated in light of the intrinsic evidence. *Id.* at 1319.

DISCUSSION

I. Person Having Ordinary Skill in the Art

The parties agree that the relevant time period in which to determine the understanding of one of ordinary skill in the art of the '571 patent is the early 1990s because the patent was filed in 1995, as a divisional of an application filed June 4, 1993, which is a continuation of a patent filed February 8, 1991. Plaintiff's expert, Dr. Jack C. Lee, states that a person of ordinary skill in the art in the early 1990s would have an undergraduate degree in electrical engineering (or an equivalent subject), along with three to four years of post-graduate experience designing semiconductor and memory devices, or a master's degree in electrical engineering (or an equivalent subject) together with one or two years of post-graduate experience designing semiconductor and memory devices. Dr. Lee states that this description is approximate, and that a higher level of education or skill could make up for less experience, and vice versa. Dkt. No. 72-2 at ¶ 20.

Defendant's expert, Mr. Joseph McAlexander, asserts that a person of ordinary skill in the art ("POSITA") in the early 1990s would have a bachelor's degree in computer engineering, electrical engineering, or a closely related field, along with at least two to three years of experience in the development and use of memory devices and systems. Dkt. No. 78-1 at ¶ 26. Mr. McAlexander asserts that a person holding an advanced degree in the relevant fields would require less experience, for example one to two years, in the development and use of memory devices and systems. *Id.* Mr. McAlexander states that although he believes a POSITA would not necessarily require as much education and/or experience as Dr. Lee asserts, "[n]evertheless, I find my proposed level of skill and Dr. Lee's proposed level of skill to be substantially the same; and my opinions about the proper construction of the disputed claim terms remain unchanged even if Dr. Lee's proposed level of skill were applied." *Id.* ¶ 27.

The Court finds that the parties' proposed POSITAs are substantially the same, and adopts plaintiff's definition.

II. 35 U.S.C. § 112(f) Means-Plus-Function

Means-plus-function terms are governed by 35 U.S.C. § 112(f), which states:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.[1]

Under this "provision, an applicant can describe an element of his invention by the result accomplished or the function served, rather than describing the item or element to be used (e.g., 'a means of connecting Part A to Part B,' rather than 'a two-penny nail')." *Warner–Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 27 (1997). When using the means-plus-function format, "[t]he applicant must describe in the patent specification some structure which performs the specified function." *Valmont Industries, Inc. v. Reinke Manufacturing Co., Inc.*, 983 F.2d 1039, 1042 (Fed. Cir. 1993). "The first step in construing such a limitation is a determination of the function of the means-plus-function limitation. The next step is to determine the corresponding structure described in the specification and equivalents thereof. Structure disclosed in the specification is 'corresponding' structure only if the specification . . . clearly links or associates that structure to the function recited in the claim." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001) (internal quotations and citations omitted). It is therefore not enough that structures be able to perform the corresponding function if they are not "clearly linked" in the specification. *Id.* "The 'cost' of using a § 112(f) function statement, especially if done unintentionally, is that the scope of the claim is restricted to the particular structures or acts disclosed in the specification, as well as their equivalents." *Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, No. IP96–1718–C–H/G, 2000 WL 1765358, at *11 (S.D. Ind. Nov. 29, 2000) (citing *Personalized Media Commc'ns, LLC v. International Trade Comm'n*, 161 F.3d 696, 703 (Fed. Cir. 1998)).

[1] As do the parties, this Order uses the terms § 112 ¶ 6 and § 112(f) interchangeably.

A. Agreed Upon § 112(f) Means-Plus-Function Terms

The parties agree that terms 4, 9, and 13[2] are means-plus-function terms subject to § 112(f). All three terms are found in Claim 1:

> 1. A multi-level memory device comprising:
>
> An electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;
> ***memory cell programming means for programming said multi-level memory cell in accordance with said input information***;
> ***reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information***, each of said reference voltages corresponding to a different one of said predetermined memory states; and
> ***comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information***.

'571 Patent at 12:6-26 (emphasis added).

1. Term 4: "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information" (Claim 1)

Plaintiff	Defendant
Function: selecting one of a set[3] of reference voltages in accordance with the input information Structure: selection circuit [including but not limited to verify reference select circuit (222), shown in Fig. 8 and described at 8:24-43 and 8:66-9:7, having as its input 2 or more output bits from an input latch/buffer circuit (224), shown in Fig. 8	Function: selecting one of a plurality of reference voltages in accordance with the input information Structure: verify reference select circuit (222), shown in Fig. 8 and described at 8:24-43 and 8:66-9:7, having as its input 2 or more output bits from an input latch/buffer circuit (224), shown in Fig. 8 and described at 8:40-43, and having as its

[2] In their claim construction briefing, the parties adopted a numbering system for the terms at issue. In the interest of consistency, the Court's order uses the same system.

[3] At the claim construction hearing, plaintiff's counsel stated that the claim language "plurality" was acceptable.

and described at 8:40-43, and having as its output an analog voltage reference signal] and all engineering equivalents thereof	output an analog voltage reference signal

The parties disagree about the structure to perform the function of "selecting one of a plurality of reference voltages in accordance with the input information." Plaintiff's expert states that the corresponding structure need only include a selection circuit because a "person having ordinary skill in the art would consider the disclosure of the 'selection circuit' more than adequate to teach structures that could be implemented to carry out the claimed function." Dkt. No. 72-2 at ¶ 36. Plaintiff contends that defendant's proposed structure unnecessarily limits the term by foreclosing an embodiment that uses a digital comparator, and by incorporating a structure from the written description beyond what is necessary to perform the claimed function.

Defendant argues that the structure should be limited to the "verify reference select circuit" embodied in Figure 8 of the patent, having two or more input bits from an input latch/buffer circuit and having as its output an analog voltage reference signal. Defendant contends that plaintiff's "selection circuit" structure never appears in the '571 patent, and that the structure in Figure 8 "clearly links . . . to the function recited in the claim." Dkt. No. 75 at 16:19-26 (citing *Saffran v. Johnson & Johnson*, 712 F.3d 549, 562 (Fed. Cir. 2013)).

The Court agrees with defendant that plaintiff's proposed "selection circuit" cannot be the corresponding structure because the specification does not specifically disclose and tie that structure to the disclosed function. Although plaintiff asserts that a POSITA would understand that a selection circuit is the corresponding structure because the specification mentions "select circuit" and examples of select circuits are shown in Figure 5 of the patent, the Federal Circuit has held that "[a] patentee cannot avoid providing specificity as to structure simply because someone of ordinary skill in the art would be able to devise a means to perform the claimed function." *Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1385 (Fed. Cir. 2009); *see also Saffran*, 712 F.3d at 562-63 ("Under § 112, ¶ 6, the question is not what structures a person of ordinary skill in the art would know are capable of performing a given function, but what structures are specifically disclosed and tied to that function in the specification."). Here, the term "selection

circuit" never appears in the '571 patent, and Figure 5's examples of several select circuits do not clearly associate those structures with the disclosed function.

The Court agrees with defendant that the specification clearly links the verify reference select circuit to the function recited in the claim. *See* '571 patent at 8:24-43; 8:66-9:7. However, the Court declines to adopt the remainder of defendant's proposal regarding inputs and output. There is nothing about the function "selecting one of a plurality of reference voltages in accordance with the input information" that requires "having as its output an analog voltage reference signal." In addition, defendant's proposal to include an analog output would exclude a digital embodiment that is disclosed by the specification. *See id*. at 9:60-65; 11:49-58. The Court also finds it unnecessary to include "having as its input 2 or more output bits from an input latch/buffer circuit" as part of the disclosed structure. Defendant does not explain why it is necessary to include this language to define the structure, nor does defendant respond to plaintiff's assertion that the input signals are not structural. *See In re Nuijten*, 500 F.3d 1346, 1355 (Fed. Cir. 2007) ("A transitory signal made of electrical or electromagnetic variances is not made of 'parts' or 'devices' in any mechanical sense. While such a signal is physical and real, it does not possess concrete structure in the sense implied by these definitions."). The specification states that the "verify reference select circuit" is "controlled by the 2-output bits from a 2-bit input latch/buffer circuit," '571 patent at 8:41-42, and further explains how the reference voltage is chosen based on the memory state to which it is to be programmed. *Id*. at 8:29-34. Thus, the verify reference select circuit disclosed in the specification is selecting one of a plurality of reference voltages "in accordance with the input information," and it is unnecessary to include language regarding the inputs when defining the structure.

For the foregoing reasons, the Court adopts the plain language function of "selecting one of a plurality of reference voltages in accordance with the input information" with the corresponding structure of a verify reference select circuit.[4] The Court does not limit the structure

[4] The parties agreed at the hearing that all terms construed under § 112(f) include equivalent structures, and not "engineering equivalents."

to the specific structures disclosed in Figure 8, and thus the verify reference select circuit may include, but is not limited to, the structure designated as "222" in Figure 8.[5]

2. Term 9: "memory cell programming means for programming said multi-level memory cell in accordance with said input information" (Claim 1)

Plaintiff	Defendant
Function: programming the multi-level memory cell in accordance with the input information Structure: timing circuitry, a program voltage switch [including but not limited to program voltage switch (220), shown in Fig. 8 and described at 8:46-57, having as its inputs (1) an enable/disable signal from an analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, and (2) a program/verify timing pulse from program/verify timing circuitry (208), shown in Fig. 8 and described at 8:53-57, and having as its outputs (1) a bitline and (2) a wordline], and all engineering equivalents thereof	Function: programming the multi-level memory cell in accordance with the input information Structure: program voltage switch (220), shown in Fig. 8 and described at 8:46-57, having as its inputs (1) an enable/disable signal from an analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, and (2) a program/verify timing pulse from program/verify timing circuitry (208), shown in Fig. 8 and described at 8:53-57, and having as its outputs (1) a bitline and (2) a wordline

The parties agree that the function is "programming the multi-level memory cell in accordance with the input information." Plaintiff argues that the corresponding structure consists of timing circuitry and a program voltage switch, which includes but is not limited to defendant's proposal. Plaintiff contends that defendant's proposed structure once again limits the term's structure beyond what is necessary to perform the claimed function because it excludes a separate embodiment using digital comparator, and risks exclusion of another implementation the specification discloses, the Fowler-Nordheim tunneling ("FNT") method.

Defendant identifies the program voltage switch in Figure 8, with its corresponding inputs and outputs, as the structure in the specification "clearly linked" to the claimed function.

[5] Similarly, the other constructions adopted in this order are not limited to the precise structures identified in Figure 8.

Defendant argues, and the Court agrees, that the patent describes the programing of the memory cell through bit line and word line voltages, which are both provided by the program voltage switch. *See* '571 patent at 10:17-37 (The "program voltage switch 220" outputs "bit line and word line program voltage outputs" during a "programming process" to "add charge to the floating gate of the memory cell."). In addition, the specification states that the programming process begins when the program voltage switch receives a "PGM timing pulse" from "timing circuit 208," which is input to the "program voltage switch 220." *Id*. In response to this pulse, the bit line and word line exert programming pulses on the cell to be programmed. *Id*.

Further, defendant's expert explains how the separate embodiment of the FNT method mentioned in the specification is not foreclosed by a structure having as its outputs both a bit line and word line. Dkt. No. 78-1 at ¶ 34. Plaintiff's expert also states that "[a]nyone skilled in the art will realize that each terminal of the memory cell will need specific voltages applied as a Programming Signal. Depending on the type of programming technique used (Fowler-Nordheim tunneling or Hot Electron injection) the Word Line and the Bit Line receive Programming Signals of different voltage Levels." Dkt. No. 72-2 at ¶ 44.

However, the Court disagrees with defendant's proposal of including in the structure the inputs from an enable/disable signal from an analog comparator circuit. This proposal contradicts the specification's disclosure of an alternate embodiment containing a "digital comparator." *See* '571 Patent at 9:64-65, 11:49-50 ("FIG. 8 may also use a digital comparator rather than the analog comparator 202 shown in FIG. 8."). In addition, the inputs from the comparator are not used specifically for programming the memory cell. The specification provides that between programming pulses, a "verify cycle" is used to compare the bit line voltage to a reference voltage and verify whether the memory cell has achieved the desired state. When the desired state is achieved, the comparator sends a "disable signal on signal line 204" to the "program voltage switch 220" to end the programming process. Thus, although the inputs from the comparator allow the programming to proceed or end the programming, the inputs from the comparator are not performing the programming function.

Although plaintiff argues that one having ordinary skill in the art only needs a program voltage switch and timing circuitry to carry out the claimed function, "[t]he 'cost' of using a § 112(f) function statement . . . is that the scope of the claim is restricted to the particular structures or acts disclosed in the specification, as well as their equivalents." *Cardiac Pacemakers*, 2000 WL 1765358, at *11 (citing *Personalized Media*, 161 F.3d at 703). As such, the Court adopts the structure of program/verify timing circuitry and a program voltage switch having its outputs (1) a bit line and (2) a word line.

3. Term 13: "comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information" (Claim 1)

Plaintiff	Defendant
Function: comparing a voltage of said multi-level memory cell with the selected reference voltage, and further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information Structure: a comparator [including but not limited to analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, having as its inputs (1) a voltage reference level signal from a verify reference select circuit (222), shown in Fig. 8 and described at 8:24-43 and 8:66-9:7, and (2) a bitline voltage from a pull-up circuit, shown in Fig. 8, and having as its output an enable/disable signal] and all engineering equivalents thereof	Function: comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to the input information Structure: analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, having as its inputs (1) a voltage reference level signal from a verify reference select circuit (222), shown in Fig. 8 and described at 8:24- 43 and 8:66-9:7, and (2) a bitline voltage from a pull-up circuit, shown in Fig. 8, and having as its output an enable/disable signal

The parties generally agree[6] on the function claimed. However, defendant argues that the structure is limited to an analog comparator circuit, having the same implementation, inputs, and outputs as item 202 in Figure 8. *See* Dkt. No. 76 at 15:5-7; Dkt. No. 75 at 26:9-13. Plaintiff contends that defendant describes more structure than is necessary to carry out the claimed function. Namely, plaintiff argues that only the comparator is necessary to carry out the claimed function, and that limiting the comparator to analog improperly excludes a digital embodiment. *Id.*; Dkt. No. 76-6 at ¶ 21-27 (demonstrating several alternate embodiments utilizing a digital comparator). Plaintiff also argues that signals and voltages are not structural.

"[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claim [term] to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). As discussed *supra*, the specification discloses a digital embodiment: "FIG. 8 may also use a digital comparator rather than the analog comparator 202 shown in FIG. 8." *See* '571 Patent at Fig. 8, 9:64-65, 11:49-50. As such, defendant has not shown why the comparator structure should be limited to the analog comparator with the same configuration as embodied in Fig. 8. *See Tex. Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1202 (Fed. Cir. 2002); *Teleflex, Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002).

The Court finds that defendant's statement of the function is clearer than plaintiff's, and therefore holds that the function is "comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to the input information." The Court agrees with plaintiff that the corresponding structure to perform this function is the comparator. Defendant has not shown why the structure should also be defined to include signals and voltages.

[6] Although defendant replaces the word "said" for the word "the" in the term's recited function, the parties do not address whether the change creates any material difference.

B. Disputed § 112(f) Means-Plus-Function Terms

The parties dispute whether claims 9, 12, and 30 contain means-plus-function terms subject to § 112(f). The burden of proof that a disputed claim is subject to § 112(f) rests with the party asserting the means-plus-function construction. *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1372 (Fed. Cir. 2003). While the use of the word "means" creates a presumption of a means-plus-function term, it is not by itself sufficient. *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1347 (Fed. Cir. 2002) (the "mere use of the word 'means' after a limitation, without more, does not suffice to make that limitation a means-plus-function limitation."). The presumption is rebutted if the claim recites sufficient structure to perform the claimed function. *Id.*; *Cole v. Kimberly–Clark Corp.*, 102 F.3d 524, 531 (Fed. Cir. 1996).

Conversely, "the failure to use the word 'means' also creates a rebuttable presumption—this time that § 112, para. 6 does not apply." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015). In *Williamson*, the Federal Circuit overruled prior case law and held that the rebuttable presumption that § 112(f) does not apply is not strong, and held that "[w]hen a claim term lacks the word 'means,' the presumption can be overcome and § 112, para. 6 will apply if the challenger demonstrates that the claim term fails to 'recite sufficiently definite structure' or else recites 'function without reciting sufficient structure for performing that function.'" *Id.* at 1349 (quoting *Watts v. XL Sys., Inc.*, 232 F.3d 877, 880 (Fed. Cir. 2000)). The claim term recites definite structure if "the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Id.* (citing *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996)). Because none of the disputed means-plus-function terms contain the word "means," the defendant must overcome the rebuttable presumption that § 112(f) does not apply by showing that the claim term does not recite definite structure understood by a person of ordinary skill in the art.

Claim 9 includes the disputed terms as follows:

> 9. Multi-level memory apparatus, comprising:
>
> An electrically alterable non-volatile memory cell having more than two predetermined memory states;
> ***a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a***

> ***memory state to which said memory cell is to be programmed***, each reference signal corresponding to a different memory state of said memory cell;
>
> **a *programming signal source which applies a programming signal to said memory cell***; and
>
> ***a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information***.

'571 patent at 13:1-15.

Claims 12 and 30 are largely similar to claim 9, except they contain terms 10 and 15 in place of the last "comparator" recitation in claim 9. *See id.* at 13:22-37 (claim 12 containing term 15: "a verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal"); *id.* at 15:10-22 (claim 30 containing term 10: "a control device to control the application of said programming signal to said memory cell based on the selected reference signal").

1. Terms 2-3: "selecting device which selects one of a plurality of [predetermined][7] reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" (Claims 9, 12, 30)

Plaintiff	Defendant
"selection circuitry that selects one of a set of [predetermined] reference signals corresponding to a memory state to which the memory cell is to be programmed, and engineering equivalents thereof" If it is determined that this term is subject to 35 U.S.C. § 112, ¶ 6: Function: selecting one of a set of [predetermined] reference signals in accordance with information indicating a memory state to which the memory cell is	Claim limitation as subject to 35 U.S.C. § 112, ¶ 6: Function: selecting one of a plurality of [predetermined] reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed Structure: verify reference select circuit (222), shown in Fig. 8 and described at 8:24-43 and 8:66-9:7, having as its input 2 or more output bits from an input latch/buffer

[7] This disputed phrase appears in identical form in claims 9, 12, and 30, except that claim 9 further specifies that the reference signals are "predetermined." The parties' proposed constructions for the claim terms in these claims are consistent, except that the proposed constructions for claim 9 contain the adjective "predetermined."

to be programmed Structure: selection circuit [including but not limited to verify reference select circuit (222), shown in Fig. 8 and described at 8:24-43 and 8:66-9:7, having as its input 2 or more output bits from an input latch/buffer circuit (224), shown in Fig. 8 and described at 8:40-43, and having as its output an analog voltage reference level signal] and all engineering equivalents thereof	circuit (224), shown in Fig. 8 and described at 8:40-43, and having as its output an analog voltage reference level signal

Plaintiff argues that this term is not subject to § 112 ¶ 6 because the patent's drafter refrained from using the words "means for," and the patentee used the means drafting language for terms 4, 9, and 13 addressed *supra*. Plaintiff also cites the expert declaration of Dr. Jack Lee, who states that "a POSITA would understand this term refers to a circuit that selects reference signals for verification of the charge stored in a multi-level cell (i.e., a desired memory state)." Dkt. No. 76-6 ¶ 10. Dr. Lee states that one example of a "selecting device" is a multiplexer. Dkt. No. 72-2 at ¶ 37.

Defendant argues that the term "selecting device" is not recognizable to one having ordinary skill in the art, and defendant's expert asserts that the "term does not convey sufficiently definite structure." Dkt. No. 75 at 14:13-16; Dkt. No. 78-1 at ¶ 65. Defendant argues that this claim term recites the same function corresponding to the "reference voltage selecting means" recited in claim 1 (designated as term 4 by the parties): "select[ing] one of a plurality of reference signals in accordance with information," but that this term fails to recite any physical or structural component beyond the claimed function. Defendant contends that the term "device" is a well-known, non-structural, nonce word. *See Robert Bosch*, 769 F.3d at 1099 ("[T]his court has found the word 'device' to be a non-structural, 'nonce' word."). Defendant argues that this claim term should be construed with means-plus-function treatment, and defendant proposes the same corresponding structure and similar function as term 4 recited in claim 1.

The Court concludes that terms 2 and 3 fail to recite sufficiently definite structure to perform the function of selecting one of a plurality of [predetermined] reference signals in

accordance with information indicating a memory state to which the memory cell is to be programmed. The Court agrees with defendant that "selecting device" is a generic term. Plaintiff does not dispute that "device" is a nonce word devoid of specific structure. *See Williamson*, 792 F.3d at 1350 (quoting *Mass. Inst. of Tech. & Elecs. For Imaging, Inc. v. Abacus Software*, 462 F.3d 1344, 1354 (Fed. Cir. 2006) ("Generic terms such as . . . 'device,'" are "nonce words that reflect nothing more than verbal constructs . . . used in a claim in a manner that is tantamount to using the word 'means' because they 'typically do not connote sufficiently definite structure' and therefore may invoke § 112, para. 6."). Adding the modifier "selecting" does not impart any structural significance to the term, and there is nothing in the written description that discloses structure for the selecting device. *Cf. Greenberg*, 91 F.3d at 1583 (holding "detent mechanism" had a structure "generally understood . . . in the mechanical arts, even though the definitions are expressed in functional terms."). Plaintiff cites an engineering textbook[8] which discusses multiplexors in support of its argument that a POSITA would understand "selecting device" to have sufficiently definite structure. *See* Dkt. No. 76-3. However, "merely listing examples of possible structures is insufficient to avoid invocation of § 112, ¶ 6." *Robert Bosch, LLC v. Snap On Inc.*, 769 F.3d 1094, 1101 (Fed. Cir. 2014).

Accordingly, because defendant has rebutted the presumption, this Court will construe this term as a means-plus-function term subject to § 112, ¶ 6. The parties' arguments regarding the corresponding structure mirror those with regard to term 4. The Court adopts the same function and structure for terms 2 and 3 as it did for term 4, and construes the claim as having the structure of the verify reference select circuit, pictured as example only in Fig. 8 as item 222, with the function of "selecting one of a plurality of [predetermined] reference signals that corresponds to a memory state to which the memory cell is to be programmed."

[8] The textbook is titled, "An Engineering Approach to Digital Design," authored by William I. Fletcher, edited by Virginia Huebner et al. and published in 1980.

2. Terms 7-8: "programming signal source [which applies/to apply] a programming signal to said memory cell" (Claims 9, 12, 30)

Plaintiff	Defendant
Plain meaning; or, "circuitry [that provides/to apply] a pulse for programming a memory cell" If it is determined that this term is subject to 35 U.S.C. § 112, ¶ 6: Function: applying a programming signal to the memory cell Structure: a program timing circuit, a program voltage circuit [including but not limited to program voltage switch (220), shown in Fig. 8 and described at 8:46-57, having as its inputs (1) an enable/disable signal from an analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, and (2) a program/verify timing pulse from program/verify timing circuitry (208), shown in Fig. 8 and described at 8:53-57, and having as its outputs (1) a bitline and (2) a wordline], and all engineering equivalents thereof	Function: programming the multi-level memory cell in accordance with the input information Structure: program voltage switch (220), shown in Fig. 8 and described at 8:46-57, having as its inputs (1) an enable/disable signal from an analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, and (2) a program/verify timing pulse from program/verify timing circuitry (208), shown in Fig. 8 and described at 8:53-57, and having as its outputs (1) a bitline and (2) a wordline If it is determined that this term is not subject to 35 U.S.C. § 112, ¶ 6, Micron proposes: "program voltage switch having as its inputs an enable/disable signal and a program/verify timing pulse, as shown in Fig. 8, and having as its outputs a bitline and a wordline which programs the memory cell in accordance with input information"

Plaintiff argues that the structure of a "programming signal source" is known to a person having ordinary skill in the art. Plaintiff's expert cites two U.S. Patents and the Fletcher engineering textbook, which discusses programming using an outside signal. *See* Dkt. No. 78-1 at ¶ 79; Dkt. No. 76-6 at ¶ 12. One of the patents cited by plaintiff's expert contains the disputed phrase in its title, "Programming Signal Source and Calibration Data for a Speedometer/Tachometer with Calibration Switches," while the other describes how a "primary transducer array acts as a coherent signal source." *See* Dkt. No. 76-6 at ¶ 12 (citing U.S. Patent No. 5,018,087 (filed Nov. 3, 1989); U.S. Patent No. 6,536,440 (filed Oct. 17, 2000)). In further support of the contention that a person of ordinary skill in the art would recognize a "programming signal source," plaintiff cites two more patents relevant in the art, one entitled "Apparatus and Method for Electronically Programming Nodal Identifications," which in its

Abstract discusses "programming signals" that "program each cell." *See* Dkt. No. 76 at 8:23-24; U.S. Patent No. 5,233,346 at abstract, 8:32-32 (filed Aug. 3, 1993).

Plaintiff also contends that because the words "programming," "signal," and "source" are, on their own, recognizable by one of ordinary skill in the art, together they contain sufficient structure. Defendant does not attempt to rebut this argument. Indeed, the definition of each word is relevant to the electrical arts. *See* Webster's New World Dictionary 1075, 1248, 1282 (3d college ed. 1988) (defining the words "programming" as "set[ting] the program of (an electronic device);" "signal" as "the electrical impulses . . . transmitted or received; and "source" as "the point or thing from which light rays, sound waves, etc. [i.e. signals] emanate"). *See Greenberg*, 91 F.3d at 1583 ("Dictionary definitions make clear that the noun 'detent' denotes a type of device with a generally understood meaning in the mechanical arts, even though the definitions are expressed in functional terms."). The Court concludes that the phrase "programming signal source" has a recognizable structure in the electrical arts, and that defendant has not met its burden of overcoming the presumption that § 112(f) does not apply.

Defendant's proposed alternative construction if § 112(f) does not apply once again attempts to limit the term to the embodiment of Figure 8. However, "it is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claim[term] to be so limited." *Liebel-Flarsheim*, 358 F.3d at 913. Defendant has not overcome the presumption that the term is construed using its plain and ordinary meaning and this Court construes the claim accordingly: "programming signal source which applies/to apply a programming signal to the memory cell." *See Tex. Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1202 (Fed. Cir. 2002); *Teleflex*, 299 F.3d at 1325.

3. Term 10: "control device to control the application of said programming signal to said memory cell based on the selected reference signal" (Claim 30)

Plaintiff	Defendant
"circuitry that controls whether charge will be transferred onto the floating gate of the memory cell during a programming process based on the selected reference signal" If it is determined that this term is subject to 35 U.S.C. § 112, ¶ 6: Function: controlling the application of said programming signal to said memory cell based on the selected reference signal Structure: a comparator [including but not limited to program voltage switch (220), shown in Fig. 8 and described at 8:46-57, having as its inputs (1) an enable/disable signal from an analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, and (2) a program/verify timing pulse from program/verify timing circuitry (208), shown in Fig. 8 and described at 8:53-57, and having as its outputs (1) a bitline and (2) a wordline], and all engineering equivalents thereof	Function: controlling the application of the programming signal to the memory cell based on the selected reference signal Structure: program voltage switch (220), shown in Fig. 8 and described at 8:46-57, having as its inputs (1) an enable/disable signal from an analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, and (2) a program/verify timing pulse from program/verify timing circuitry (208), shown in Fig. 8 and described at 8:53-57, and having as its outputs (1) a bitline and (2) a wordline If it is determined that this term is not subject to 35 U.S.C. § 112, ¶ 6, Micron proposes: "program voltage switch having as its input an enable/disable signal and a program/verify timing pulse, as shown in Fig. 8, and having as its outputs a bitline and a wordline to control the application of the programming signal to the memory cell based on the selected reference signal"

Plaintiff argues that a person of ordinary skill in the art would understand a "control device" to recite sufficiently definite structure, citing its expert witness who introduces a chapter in an engineering textbook entitled "System Controllers." Dkt. No. 76 at 25-28; Dkt. No. 76-6 at ¶ 14; Dkt. No. 76-3 at § 7-2. Although the chapter does not contain the term "control device," it provides an understandable structure for the term. *See* Dkt. No. 76-3 at § 7-2 (defining a "system controller" as "a special sequential machine . . . designed to interpret system level control input sequences and in turn to generate system level output sequences"). This claim is buttressed by the definition of "control" as "an instrument or apparatus to regulate a mechanism; a device used to adjust or control." *See* Webster's New World Dictionary 303 (3d college ed. 1988).

Aside from asserting that "control device" is a nonce phrase, defendant does not advance any specific arguments showing that a POSITA would not understand a "control device" to have specific structure. Defendant also cites *Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361 (Fed. Cir. 2012), in which the Federal Circuit found that the "recitation of 'control device' provides no more structure than the term 'control means' itself, rather it merely replaces the word 'means' with the generic term 'device.'" *Id*. at 1363-64. However, the patent in *Ergo* belonged to a different art and was associated with the control of fluids. *See id.* at 1361. Here, the patent belongs to the electrical arts, and plaintiff's expert has provided support that the structure of a "control device" is well known in the field. The Court finds that defendant has not rebutted the presumption that § 112, ¶ 6 does not apply.

Next, the parties present alternate constructions if § 112(f) does not apply. Plaintiff argues that its construction "accords with the specification's full teachings of how the programming signal is applied to a memory cell." Dkt. No. 72 at 26:7-9. However, plaintiff does not address why it proposes to define the "control device" under the broader construction of "circuitry," nor does it respond to defendant's contentions against this construction. *See* Dkt. No. 75 at 22:11-13. Defendant, on the other hand, construes the term according to the specific embodiment of Figure 8 because, for instance, "an enable/disable signal is involved in the application of a programming signal to a memory cell." *See* Dkt. No. 75 at 22:16-18.

However, it is improper to read limitations from a specification's embodiment into the claim. *See Liebel-Flarsheim*, 358 F.3d at 913. Therefore, the term cannot be limited to the embodiment of Fig. 8, but there is no reason why the "control device," as a structure known in the arts, should be construed as "circuitry" either. For those reasons, this Court construes the term according to its plain meaning: "control device to control the application of the programming signal to the memory cell based on the selected reference signal."[9]

[9] The Court replaces the word "said" with "the" so that the construction may be more understandable to a jury.

4. Term 14: "comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information" (Claim 9)

Plaintiff	Defendant
"circuitry that compares a signal corresponding to the state of the memory cell with the selected reference signal to verify whether the memory cell is programmed to the state indicated by the input information" If it is determined that this term is subject to 35 U.S.C. § 112, ¶ 6: Function: comparing a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information Structure: a comparator [including but not limited to analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, having as its inputs (1) a voltage reference level signal from a verify reference select circuit (222), shown in Fig. 8 and described at 8:24-43 and 8:66-9:7, and (2) a bitline voltage from a pullup circuit, shown in Fig. 8, and having as its output an enable/disable signal], and all engineering equivalents thereof	Function: comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to the input information Structure: analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, having as its inputs (1) a voltage reference level signal from a verify reference select circuit (222), shown in Fig. 8 and described at 8:24-43 and 8:66-9:7, and (2) a bitline voltage from a pull-up circuit, shown in Fig. 8, and having as its output an enable/disable signal If it is determined that this term is not subject to 35 U.S.C. § 112, ¶ 6: plain and ordinary meaning In the alternative, this term is indefinite

Plaintiff argues that a comparator has a structure well known to persons holding ordinary skill in the art and that term 14 should be construed based on its plain and ordinary meaning. Defendant does not address whether a person having ordinary skill in the art would understand the structure of a comparator. Instead, defendant argues that plaintiff's proposed constructions are unreasonably broad and lack support. Defendant relies on the previous term 13, which contains a similar function and structure but with the "means . . . for" wording, to contend that term 14 should receive the same § 112(f) construction. However, defendant fails to address the rebuttable

presumption that § 112(f) does not apply if the "means . . . for" language is not present in the term. *See Williamson*, 792 F.3d at 1349.

Here, in order for § 112(f) to apply, defendant must show that the claim term fails to recite definite structure. *See id.* While plaintiff has cited two sections in different engineering textbooks that focus on the functionality of a comparator structure, defendant has provided no rebuttal to that point. *See* Docket No. 72-5 at § 26.1 (entitled "Basic CMOS Comparator Design"); Dkt. No. 76-3 at § 4-4 (entitled "Comparators"). Moreover, a comparator is defined in the dictionary as "any of various instruments, esp. in electronics, for comparing some measurement, as of length, brightness, voltage, etc., with a fixed standard." Webster's New World Dictionary 283 (3d college ed. 1988). The definition indicates that a comparator, as a noun, is defined by its function and is generally known in the electrical arts. Similarly, in *Greenberg*, the court concluded that even though the definition of "detent" was expressed in functional terms, the definition made clear that the noun "denotes a type of device with a generally understood meaning in the mechanical arts." *See* 91 F.3d at 1583 ("Many devices take their names from the functions they perform. The examples are innumerable, such as 'filter,' 'brake,' 'clamp,' 'screwdriver,' or 'lock.'").

Therefore, the Court construes the term according to its plain and ordinary meaning: "comparator which compares a signal corresponding to the state of a memory cell with the selected reference signal to verify whether the memory cell is programmed to the state indicated by the input information."

5. Term 15: "verifying device which detects a parameter indicating the state of said memory cell and which verifies whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal" (Claim 12)

Plaintiff	Defendant
"circuitry that detects an indicator of the state of the memory cell and verifies whether the memory cell is programmed to the state indicated by the input information by comparing the indicator to the selected reference signal"	Function: comparing a voltage of the multi-level memory cell with the selected reference voltage, and for further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to

If it is determined that this term is subject to 35 U.S.C. § 112, ¶ 6: Function: detecting an indicator of the state of the memory cell and verifying whether the memory cell is programmed to the state indicated by the input information by comparing the indicator to the selected reference signal Structure: a comparator and all engineering equivalents thereof	the input information Structure: analog comparator circuit (202), shown in Fig. 8 and described at 8:26-48 and 8:66-9:3, having as its inputs (1) a voltage reference level signal from a verify reference select circuit (222), shown in Fig. 8 and described at 8:24-43 and 8:66-9:7, and (2) a bitline voltage from a pull-up circuit, shown in Fig. 8, and having as its output an enable/disable signal If it is determined that this term is not subject to 35 U.S.C. § 112, ¶ 6: "analog comparator circuit having as its inputs a voltage reference level signal and a bitline voltage, as shown in Fig. 8, and having as its output an enable/disable signal which compares a voltage of the multi-level memory cell with the selected reference voltage, and which generates a control signal indicating whether the state of said multi-level memory cell is the state corresponding to the input information" In the alternative, this term is indefinite

Defendant argues that the term "verifying device" is not recognizable to one having ordinary skill in the art, and defendant's expert asserts that the term does not convey sufficiently definite structure. Dkt. No. 78-1 at ¶ 119. Plaintiff contends that a "verifying device" would be understood by a POSITA. Dkt. No. 76 at 18:22-25. As support, plaintiff cites the Fletcher engineering textbook, which discusses comparators with no mention of a "verifying device." *Id.*; Dkt. No. 76-3 at § 4-4 (entitled "Comparators").

The Court concludes that term 15 fails to recite sufficiently definite structure to perform the function of detecting a parameter indicating the state of a memory cell and verifying whether the memory cell is programmed to the state indicated by the input information based on the detected parameter and the selected reference signal. The Court agrees with defendant that "verifying device" is a generic term that does not disclose any structure or physical component.

Accordingly, because defendant has rebutted the presumption, this Court will construe this term as a means-plus-function term subject to § 112, ¶ 6. The parties disagree on both the function and structure of the term. Defendant argues for a functional construction that is more limited than the claim's language because it construes the recited "signals" as "voltages" and adds the limitation of "generating a control signal." *See* Dkt. No. 75 at 28:18-29:1. Defendant provides no explanation for limiting the claim's function, merely arguing that plaintiff's function is unsupported by the intrinsic record because, for example, the word "indicator" is not present in the patent's claim or specification. *See id.* at 30:1-7. Plaintiff, on the other hand, contends that it is adopting the function as recited in the claim's term.

The Federal Circuit has warned against adopting a function different from what is explicitly recited in the claim. *See Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999); *Generation II Orthotics Inc. v. Med. Tech. Inc.*, 263 F.3d 1356, 1364–65 (Fed. Cir. 2001) ("When construing the functional statement in a means-plus-function limitation, we must take great care not to impermissibly limit the function by adopting a function different from that explicitly recited in the claim."). Therefore, the Court adopts the function recited in the claim: detecting a parameter indicating the state of a memory cell and verifying whether the memory cell is programmed to the state indicated by the input information[10] based on the detected parameter and the selected reference signal. The parties each argue for the same structures as for term 13. For the same reasons, the Court adopts the structure of a comparator.

III. Remaining Terms

The parties dispute the construction of terms 1, 5, 6, 11, 12, and 16. These terms are found in Claims 9, 42 and 45. Representative Claim 45 is as follows:

> 45. A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:

[10] Both parties agree on the addition of "input" before "information" in the term's function so that the programming state is indicated by the "input information." Further, this construction is consistent with the construction of term 14.

> ***selecting one of a plurality of reference signals in accordance with information indicating*** a memory state to which said memory cell is to be programmed, each reference signal corresponding to a different memory state of said memory cell;
> ***applying a programming signal to said memory cell***; and ***controlling the application of said programming signal to said memory cell based on the selected reference signal***.

'571 Patent at 16:42-53 (emphasis added).

A. "Reference Signal/Voltage" Terms

1. Term 1: "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" (Claims 42 and 45)

Plaintiff	Defendant
"selecting one of a set[11] of reference signals that corresponds to a memory state to which the memory cell is to be programmed"	"selecting one of a plurality of analog verify signal values that corresponds to one memory state, where the memory state corresponds to the programming information"

The parties dispute whether "reference signals" should be given their plain meaning, as plaintiff argues, or should be limited to "analog verify signal values," as defendant argues. Plaintiff contends that defendant's construction should not be adopted because a person of ordinary skill in the art would understand a "signal" to be broader than a "signal value." Plaintiff's expert explains that while a signal is a continuous transfer of energy over time represented by a waveform, a signal value is only a scalar number relating to that waveform. Dkt. No. 76 at ¶¶ 4, 6. Plaintiff further argues that a person of ordinary skill in the art would understand a digital comparator to use digital signals, making defendant's construction, which limits the term to an analog implementation, incorrect.

To support the construction of the signal as analog, defendant points to the preferred embodiment in the specification that describes the signal values as analog values to be inputted into an analog comparator. *See* '571 Patent at 8:27-9:7. However, "it is improper to read

[11] At the claim construction hearing, plaintiff's counsel stated that plaintiff agreed to a construction using "plurality."

limitations from a preferred embodiment described in the specification . . . into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *DealerTrack, Inc. v. Huber*, 674 F.3d 1315, 1327 (Fed. Cir. 2012) (citation omitted). The patent's specification states that signals can be encoded as digital. *See* '571 Patent at 11:54-57 ("The verify reference voltage select 222 would provide the voltage to be encoded with the input coming from the output of the n-bit input latch/buffer . . ."). While the patent does not specifically refer to the encoding of the verify reference signals, there is no indication that the patentee intended the signals to be limited to analog. *See DealerTrack*, 674 F.3d at 1327; *Liebel-Flarsheim*, 358 F.3d at 913.

Defendant's construction also includes the adjective "verify" to differentiate between the claimed "verify reference signal" and "read reference voltages" disclosed in the specification. This differentiation is unnecessary because the read reference voltages are never disclosed as "signals" in the specification. *See, e.g.* '571 Patent at 8:23; *see also American Piledriving Equipment, Inc. v. Geoquip, Inc.*, 637 F.3d 1324, 1331 (Fed. Cir. 2001) ("[T]he role of a district court in construing claims is not to redefine claim recitations or to read limitations into claims to obviate factual questions of infringement . . ."). One of ordinary skill in the art could discern from the intrinsic record the difference between the claimed "reference signal" and disclosed "reference voltage." *See* '571 Patent at 8:2-5; *Phillips*, 415 F.3d at 1317 ("[W]hile extrinsic evidence can shed useful light on the relevant art, . . . it is less significant than the intrinsic record in determining the legally operative meaning of claim language.").

Defendant also argues against giving the last portion of the term, "to which said memory cell is to be programmed," its plain and ordinary meaning, instead proposing "where the memory state corresponds to the programming information." Plaintiff, on the other hand, adopts what is essentially the plain meaning of the remainder of the term: "to which the memory cell is to be programmed." The main difference between these proposals seems to be grammatical, not substantive. Because this difference does not change the scope of the claim, plaintiff's more concise word choice is adopted as less confusing to a jury. *See also Teleflex*, 299 F.3d at 1325

("We indulge a 'heavy presumption' that a claim term carries its ordinary and customary meaning.").

Accordingly, the Court construes "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" as "selecting one of a plurality of reference signals that corresponds to a memory state to which the memory cell is to be programmed."

2. Term 5: "reference voltage(s) . . . each of said reference voltages corresponding to a different one of said predetermined memory states" (Claim 1)

Plaintiff	Defendant
"distinct voltage(s) corresponding to a particular memory state"	"verify voltage value(s), each verify voltage value corresponding to a different one of predetermined memory states"

The parties disagree on whether the term "reference voltage(s)" should be construed as "distinct voltage(s)" or "verify voltage value(s)." Defendant contends that "verify" will distinguish the reference voltages selected by the verify reference device (item 222 in Fig. 8) from the read reference voltages selected by the sensor/encode logic circuit (items 152, 160 in Fig. 8). Plaintiff asserts that defendant is improperly seeking to limit "reference" to "verify." The Court finds that the addition of the word "verify" will help distinguish between the two types of reference voltages disclosed in the patent's specification, especially given the fact that the read reference voltages are also disclosed as simply "reference voltages." *See, e.g.* '571 Patent at 7:20-24.

Plaintiff contends that construing "reference voltage(s)" as "voltage value(s)" would confuse the terms of Claim 1 with the "voltage values" recited in Claim 2, "thus making Claim 2 superfluous or, at the very least, circular." Dkt. No. 72 at 12:5-9. The Court agrees and finds that construing "voltage(s)" as "voltage value(s)" would confuse the terms of Claim 1 with Claim 2.

Accordingly, the Court construes term 5 as "verify reference voltage(s), each verify reference voltage corresponding to a different one of the predetermined memory states."

3. Term 6: "reference signal(s) . . . each reference signal corresponding to a different memory state of said memory cell" (Claims 9, 12, 30, 42, 45)

Plaintiff	Defendant
"distinct signal(s) corresponding to a particular memory state"	"analog verify signal value(s), each analog verify signal value corresponding to a different memory states of the memory cell"

The parties disagree whether the term "reference signal(s)" should be construed as "distinct signal(s)," as plaintiff argues, or "analog verify signal value(s)," as defendant argues. Although defendant offers expert opinion that a voltage, as an analog signal value, is a type of signal, the expert admits that a signal is a broader term than voltage. *See* Dkt. No. 78-1 at ¶ 53 ("The 'reference signal(s),' however, more broadly refer to 'signals' rather than a 'voltage' . . ."). Despite the analog embodiment, depicted in Figure 8, that includes reference voltages as opposed to signals, the specification makes clear that the technology can be implemented using analog or digital signals. Construing "reference signal(s)" as "analog . . . value(s)" would unnecessarily import limitations from the specification into the claim. Because "[a] basic claim construction canon is that one may not read a limitation into a claim from the written description," the more limited construal should not be adopted. *RF Delaware, Inc. v. Pac. Keystone Techs., Inc.*, 326 F.3d 1255, 1264 (Fed. Cir. 2003) (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998)).

Moreover, just as with term 1, the addition of the word "verify" to differentiate between the claimed "reference signals" and the "reference voltages" disclosed in the specification is unnecessary because the read reference voltages are never disclosed as "signals." *See, e.g.* '571 Patent at 8:23; *see also American Piledriving*, 637 F.3d at 1331. Accordingly, the Court construes the claim according to its plain meaning: "reference signal(s), each reference signal corresponding to a different memory state of the memory cell."

B. "Programming" Terms

1. Term 11: "applying a programming signal to said memory cell" (Claims 42 and 45)

Plaintiff	Defendant
Plain meaning; or "applying a programming pulse to a terminal of the memory cell during a programming cycle"	"applying a programming signal via a bitline and a wordline to a memory cell"

Plaintiff contends that "applying a programming signal to said memory cell" should be given its plain and ordinary meaning, while defendant argues that this term should be construed according to the embodiment disclosed in Figure 8 of the specification, where the programming signal is applied to the memory cell via a bitline and a wordline. Plaintiff argues that defendant's construction includes an unnecessary limitation—that programming be done via a bitline and a wordline—that is not found in the claim language, and thus is unnecessary.

There is a heavy presumption that claim terms carry their ordinary and customary meaning. *See Tex. Digital*, 308 F.3d at 1202; Teleflex, 299 F.3d at 1325 ("We indulge a 'heavy presumption' that a claim term carries its ordinary and customary meaning."). As such, "it is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claim [term] to be so limited." *Liebel-Flarsheim*, 358 F.3d at 913. The Court concludes that defendant has not overcome the presumption that the term should be construed using its plain and ordinary meaning.

2. Term 12: "controlling the application of said programming signal to said memory cell based on the selected reference signal" (Claim 45)

Plaintiff	Defendant
Plain meaning; or "controlling the application of a pulse for transferring electrons onto the floating gate of the memory cell based on the selected reference signals"	Indefinite

Plaintiff argues that this phrase should be given its plain and ordinary meaning, or alternatively should be defined as "controlling the application of a pulse for transferring electrons onto the floating gate of the memory cell based on the selected reference signals." Defendant argues that this phrase is indefinite because the term, when read in light of the specification, fails to inform skilled artisans about the scope of the invention with reasonable certainty. Defendant does not offer an alternative construction.

In making this argument, defendant cites *Nautilus, Inc. v. Biosig Instruments, Inc*., 134 S. Ct. 2120 (2014). In *Nautilus*, the Supreme Court held that "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Id.* at 2124. Here, defendant has not included the patent's prosecution history in evidence, nor referred to it in its brief. The Court finds that on this record, defendant has not met its burden to show that this claim is indefinite. Defendant may renew its indefiniteness challenge on a fuller factual record.

The Court adopts the plain and ordinary meaning of the term.

3. Term 16: "verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal" (Claim 42)

Plaintiff	Defendant
"verifying whether the memory cell is programmed to the memory state indicated by comparing an indicator of the memory state with the selected reference signal"	"verifying the memory cell state by comparing a selected reference signal and a bitline voltage"

The parties' dispute concerns the "detected parameter" that is used to compare against the "selected reference signal" to verify whether the memory cell is programmed correctly. Plaintiff argues that the "detected parameter" should be defined as "an indicator of the memory state," while defendant argues that the "detected parameter" is a "bitline voltage."

Plaintiff contends that a "detected parameter" may encompass more than just a bitline voltage, and that defendant is seeking to improperly limit the claim to the preferred embodiment. Plaintiff also argues that defendant's construction would exclude the embodiment covered by dependent claim 43, which specifies that the detected parameter "is detected at the bit line terminal," and thus could be a voltage or a value. Plaintiff also argues that defendant's construction renders superfluous dependent claim 44, which specifies that the detected parameter is a "bit line voltage."

Defendant argues that plaintiff's proposed construction impermissibly expands the scope of the claim. Defendant cites the patent specification which, in discussing Figure 8, describes the analog comparator 202 comparing a reference signal ("[A] verify reference voltage select circuit 222 provides an analog voltage reference level signal X to one input terminal of an analog comparator 202") to a bitline voltage ("The Y signal input terminal of the analog comparator 202 is connected to the bit line output terminal 168 of the multi-level memory cell 102"). '517 Patent at 8:26-29, 8:43-45; *see also id*. at 8:66-9:3 ("The voltage threshold of memory cell 102 is then determined by using the comparator 202 to compare the bit line voltage at terminal 168 with the selected verify reference voltage from the verify reference voltage select circuit 222.").

The Court adopts plaintiff's construction and construes "verifying whether said memory cell is programmed to the state indicated by said information based on the detected parameter and the selected reference signal" as "verifying whether the memory cell is programmed to the memory state indicated by comparing an indicator of the memory state with the selected reference signal." The Court agrees with plaintiff that defendant seeks to limit the construction to the embodiment contained in Figure 8. Further, dependent claim 44 limits the "detected parameter" to "bitline voltage," and thus the "detected parameter" in independent claim 42 must be broader than "bitline voltage," or claim 44 would be superfluous. "Under the doctrine of claim differentiation, dependent claims are presumed to be of narrower scope than the independent claims from which they depend." *AK Steel Corp. v. Sollac*, 344 F.3d 1234, 1242 (Fed. Cir. 2003). This "presumption is especially strong when the limitation in dispute is the only meaningful difference between an independent and dependent claim, and one party is urging that the limitation in the dependent

claim should be read into the independent claim." *SunRace Roots Enter. Co. v. SRAM Corp.*, 336 F.3d 1298, 1303 (Fed. Cir. 2003).

CONCLUSION

For the foregoing reasons and for good cause shown, the Court hereby adopts the constructions set forth in this order.

IT IS SO ORDERED.

Dated: November 4, 2016

SUSAN ILLSTON
United States District Judge